

Inventor: H. Montgomery Manning

Title: Integrated Circuitry and a Semiconductor Processing Method of Forming a  
Series of Conductive Lines

Assignee: Micron Technology, Inc.

Docket No. MI22-2374

**INFORMATION DISCLOSURE STATEMENT**

**PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98**


In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/526,797, filed April 22, 1997. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 26 Aug 2003

By:   
James E. Lake  
Reg. No. 44,854

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2374		SERIAL NO. Filed Herewith	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT H. Montgomery Manning			
				FILING DATE Filed Herewith		GROUP 2826	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,552,628	09/1996	Watanabe			
	AB	5,585,664	12/1996	Ito			
	AC	5,583,357	12/1996	Choe			
	AD	4,418,239	11/1983	Larson			
	AE	4,693,530	09/1987	Stillie			
	AF	4,781,620	11/1988	Tengler			
	AG	4,933,743	06/1990	Thomas			
	AH	5,000,818	03/1991	Thomas			
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	AJ	5,123,325	06/1992	Turner			
	AK	5,176,538	01/1993	Hansell, III			
	AL	4,686,759	08/1987	Pals			
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes    No
	AM	JP 0097300	04/1994	Japan			
	AN	JP 054925	02/1990	Japan			
	AO						
	AP						
	AQ						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		Thomas, Michael E., "VLSI Multilevel Micro-Coaxial Interconnects for High Speed Devices", 1990, IEEE, pps. 55-58.				
	AS						
	AT						
EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

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				FILING DATE Filed Herewith		GROUP 2826
U.S. PATENT DOCUMENTS						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	4,922,323	05/1990	Potter		
	AB	5,323,048	06/1994	Onuma		
	AC	5,329,155	07/1994	Lao		
	AD	5,471,093	11/1995	Cheung		
	AE	5,028,981	07/1991	Eguchi		
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	AG	5,656,543	08/1997	Chung		
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	AK	5,451,551	09/1995	Krishman et al		
	AL	5,956,615	09/1999	Nguyen et al		
FOREIGN PATENT DOCUMENTS						
	Document Number	Date	Country	Class	Subclass	Translation
						Yes    No
	AM					
	AN					
	AO					
	AP					
	AQ					
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)						
	AR					
	AS					
	AT					
EXAMINER			DATE CONSIDERED			
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